	US ATLAS **PHASE II Upgrade** **BASIS of ESTIMATE (BoE)**	**Date of Estimate:** **11/16/2015**
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		Docdb #: XXX

WBS number: X.XX.XX	**WBS Title: DAQ Aggregator**

WBS Dictionary Definition:
Design, prototype, and build the DAQ Aggregator (DAG) board to enable the ATLAS experiment to concentrate information from the detector and trigger systems as a feed-in to a low-level global trigger processing system (L0Global or L1Global). The DAG board will receive signals from the liquid argon & tile calorimeters, L0Muon, L1Track, and L0Calo, and combines the information for transmission to L0Global and/or L1Global. Under this WBS the deliverables to ATLAS are 8 (eight) DAG boards, and the transmission and controls firmware for the board.

Estimate Type (check all that apply – see BOE Report for estimate type by activity):

___ Work Complete
___ Existing Purchase Order
___ Catalog Listing or Industrial Construction Database
___ Documented Vendor Estimate based on Drawings/ Sketches/ Specifications
_X_ Engineering Estimate based on Similar Items or Procedures
___ Engineering Estimate based on Analysis
___ Expert Opinion

Supporting Documents (including but not limited to): References the gFEX (Docdb#256)

Summary Description of this Project

A centerpiece of the ATLAS TDAQ Phase-II upgrade is a global trigger system (L0Global or L1Global) that processes entire events with low latency. The data flow for this system requires a parallel event building or aggregator layer prior to the event processing step that provides the many-to-many mapping between inputs and event processors and avoids the issues with latency and throughput associated with a switched network. The DAQ Aggregator (DAG) board is an electronics processor board that combines information from liquid argon & tile calorimeters, L0Calo, L0Muon, and L1Track. There will be between around 100 to 300 input sources to the global system, the precise number depending on whether the links from the calorimeter RODs to Global are located on the mezzanines or on the main modules. Each of these sources needs to have a route to every Event Processor. The DAG requires low-latency and high I/O which is best realized in large FPGAs. Work involved in this WBS item includes design, construction, and testing of the DAG board as well as development of input, output, and board control firmware.

Details of the Base of Estimate

This BOE covers the cost of construction of the DAQ aggregator, transmissions and controls firmware, and project management. The DAG board will be developed in three distinct phases: (1) Prototyping, (2) Pre-production and (3)

Production. The first step is critical to establish successful communications between FPGAs and with the external input/output lines. At this stage we expect to have a platform for firmware development and perform initial integration tests with other ATLAS components. The prototyping phase is divided into two steps (a) prototype 1 where only one FPGA is used, and (b) a full prototype. The second phase will be used to prepare the necessary steps for the production board, correcting problems found during the prototyping board. During the last step we will produce the DAG board proper. The deliverable to ATLAS are eight DAG boards. The fabrication cost estimate is based on the component level costs, vendor costs for board fabrication, and vendor assembly. Components costs and board fabrication & assembly are estimated on the basis of Phase-I global feature extractor (gFEX) board, now under construction.

The level of effort for the DAG board production is estimated from what was required to design and fabricate the gFEX board. Board design and layout will be made by a junior BNL engineer (1 FTE) while another junior BNL engineer (1 FTE) concentrates on the low-latency transmission and board controls firmware. An uncosted physicist will perform the project management (0.25 FTE). Five years are assumed in this projection (FY18-22). A Summary cost estimate for the DAG board prototyping, pre-production, and production is given in Table 1.

Assumptions in cost estimate:

Board Design: To estimate the level of effort required to complete this project we assume that the DAG board will be designed in house and later fabricated by a vendor. The board design, testing, and qualification will be by a BNL junior engineer (1 FTE). The level of effort was estimated on the basis of time required to design the gFEX which has similar complexity. The estimated cost for FTE was done using standard BNL rate tables.

Components: We divide the cost of components in two parts: FPGA purchase and the remaining components. The Xilinx Ultrascale+ VU13P with 128 GTY transceivers, expected in CY2017, has the highest I/O density amongst FPGA. While prices have not yet been disclosed, similar-sized previous-generation FPGA are retailing for $25-28k so we estimate $28k per FPGA. Controls will be on a Zynq MPSoC which is estimated to cost $5k. Board components and PCB are estimated at $12k based on the gFEX construction. A DAG board has 3 FPGA and 1 Zynq totaling $101k. We split the procurement into two epochs. The purchase of parts for the prototype board will be done separately from pre-production and production boards. This strategy will allow for a late decision on the FPGA to be used in the final board.

Tag	Stage	FY	Labor FTE	Labor Hrs	Labor $	M&S $	Travel $	Total $
DAG1000	*Design*	18	0.25 Jr. Eng	444	$26,062.00	$0.00	$0.00	$26,062.00
DAG1010	*Prototype 1*	19	2.0 Jr. Eng	3552	$224,460.00	$54,000.00	$11,500.00	$289,960.00
	Prototype 2	20	2.0 Jr. Eng	3552	$233,438.00	$110,000.00	$10,000.00	$353,438.00
DAG1020	*Pre-production*	21	2.0 Jr. Eng	3552	$240,442.00	$110,000.00	$10,000.00	$360,442.00
DAG1030	*Production*	22	1.0 Jr. Eng	1776	$123,827.00	$880,000.00	$5,500.00	$1,009,327.00
	Total $				$848,229.00	$1,154,000.00	$37,000.00	$2,039,229.00

Table 1 DAG board and firmware cost summary excluding the 30% contingency.

Board Fabrication: We will use external vendors to fabricate and populate the board. Upon receipt the board will be inspected and tested following the same steps for all three phases. The cost of board fabrication of $9k is estimated on the basis of the gFEX that has a similar number of layers and routing complexities.

Firmware Development: The responsibility is to develop firmware that will receive, refine, and reformat the data from the transceivers feeding the firmware that will actually perform data aggregation. Full-time equivalent for the development of firmware was estimated on the basis of similar developments made in recent years at BNL. This activity will occur primarily during the prototype and pre-production phases and will be the responsibility of a junior BNL engineer (1 FTE). The estimated cost for FTE was done using standard BNL rate tables.

Travel: Travel cost has been estimated on the basis of frequent travel between BNL and CERN. For travel with one week duration this cost is $2,500 and for a two weeks travel this cost is $3,000. Domestic travel cost is based on short trips made to visit vendors at a cost of $1,500.

Risk Analysis

Scope Risk – Probability: *High*, Impact: *Moderate*, Overall: *Moderate*

> Potential problem: The architecture for Phase-II TDAQ is not settled. This impacts the overall number of aggegrator boards needed.
>
> Mitigation: Changes in architecture will mostly impact the number of production DAG boards needed. Little impact is expected on the prototype or pre-production phases.

Schedule Risk – Probability: *Moderate*, Impact: *Low*, Overall: *Low*

> Potential problem: The scheduling for the board production should follow the overall ATLAS Phase-II TDAQ schedule. Schedule slippage on decisions will impact on the DAG project activities.
>
> Mitigation: The implementation of the final configuration will be during the pre-prototype board design and fabrication. Installation scheduling slippage may be handled by other participating institutions or supported by operations funds.

Cost Risk – Probability: *Low*, Impact: *Moderate*, Overall: *Low*

> Potential problem: There is a possibility that we may need to rework the board and new FPGAs required in this case. The FPGAs have a large number of pin count and there is a finite chance that we may damage the component during its removal. As a consequence we may need to purchase extra FPGAs.
>
> Mitigation: Cost contingency for the extra FPGA purchase has taken this fact into account.

Technical Risk – Probability: *Moderate*, Impact: *Low*, Overall: *Low*

> Potential problem: Cooling of FPGAs and other components. The lifetime of FPGAs depend on their operating temperature.
>
> Mitigation: We will perform tests with air cooling and if it's found not to be effective we will implement water cooling. Similar cooling has been developed for the ATLAS Liquid Argon Calorimeter electronics.

Contingency Analysis

Contingency is based on the estimate for the Phase-I gFEX.

M&S Contingency: 30%

The M&S contingency reflects the fact that we may need to purchase extra FPGAs and other components in case a replacement parts are needed if boards needs to be reworked during the production.

Labor Contingency: 30%
This project may require more effort in testing boards than we are currently expecting. The board is expected to be complex and the number of hours required for their testing can be larger than expected.

Total Project Contingency: 30%
The total project contingency for WBS X.XX.XX is 30%

Additional Comments

1) We assume the full eight DAG boards are constructed. Project costs decrease significantly if fewer boards are required.

2) We estimated the level of effort based on previous experiences to design and manufacture boards of similar complexity. The largest source of uncertainty in this estimate comes from the level of effort required to test the board.